AMENDMENTS TO THE SPECIFICATION:

Please replace paragraph [01] with the following two new paragraphs:

[01.1] ~~[Not Applicable]~~ The present application is a continuation of U.S. Application Serial No. 10/352,417 filed January 28, 2003 titled "Memory Cell With Fuse Element" (Attorney Docket No. 13374US02) which is a continuation of U.S. Application Serial No. 10/025,132 filed December 18, 2001 titled "Memory Cell With Fuse Element" (Attorney Docket No. 13374US01), now U.S. Patent No. 6,525,955 issued February 25, 2003, the complete subject matter of each of which is incorporated herein by reference in its entirety.

[01.2] U.S. Application Serial No. 10/352,417 is also a continuation-in-part of Patent Application No. 10/012,858 filed November 3, 2001 titled "Very Small Swing High Performance Asynchronous CMOS Static Memory (Multi-Port Register File) With Power Reducing Column Multiplexing Scheme" (Attorney Docket No. 13386US01), now U.S. Patent No. 6,639,866 issued October 28, 2003, which in turn claims priority from Provisional Application No. 60/245,913, filed November 3, 2000.

Please replace the Abstract and with the following amended Abstract:

The present invention relates to a programmable memory ~~cell~~ device and a method of setting a state for a programmable memory ~~cell~~ device. In at least one embodiment, the memory device comprises at least a level shifter adapted to standoff a high programming voltage to at least one fuse element in the memory device, wherein the high programmable voltage is used to set a state of the memory device. ~~The memory cell includes two thin gated fuses adapted to set the state of the memory cell. A level shifter device is connected to the gated fuses and is adapted to stand off a high voltage when setting the state of the memory cell. At least one switch transistor is connected to at least the level shifter device and is adapted to select at least one of the gated fuses, enabling a high voltage to be communicated thereto, thus setting the state of the memory cell.~~